IN THE CLAIMS:

Please note that all of the claims that are currently pending and under consideration in the above-referenced application are shown below, in clean form, for the sake of clarity. Also, a marked-up version of each amended claim is enclosed herewith to clearly identify each change that has been made thereto.

Please cancel claims 68-102 without prejudice or disclaimer.

Please enter the claims as follows.

1. (Amended) A semiconductor device for use in a stacked multi-chip assembly, comprising:

a semiconductor die; and

a spacer layer comprising dielectric material, formed on at least a portion of a surface of said semiconductor die, and protruding therefrom substantially a predetermined distance that said semiconductor die and an adjacent semiconductor die of said stacked multi-chip assembly are to be spaced apart from one another, said spacer layer including voids communicating with a lateral periphery thereof.

2. The semiconductor device of claim 1, wherein said spacer layer comprises a plurality of laterally discrete spacers.

3. The semiconductor device of claim 1, further comprising:

at least one discrete conductive element protruding above a surface of said semiconductor die.

4. The semiconductor device of claim 3, wherein said at least one discrete conductive element comprises one of a bond wire, a thermocompression bonded lead, and a tape-automated bond element.

5. The semiconductor device of claim 1, wherein said predetermined distance exceeds a distance a discrete conductive element protrudes above a surface of at least one of said semiconductor die and said adjacent semiconductor die.

6. The semiconductor device of claim 1, wherein said predetermined distance is about the same as or less than a distance a discrete conductive element protrudes above a surface of at least one of said semiconductor die and said adjacent semiconductor die.

7. The semiconductor device of claim 1, wherein said spacer layer covers only a portion of said surface.

8. The semiconductor device of claim 7, wherein said spacer layer comprises a pattern.

9. The semiconductor device of claim 7, wherein said spacer layer comprises randomly arranged features.

10. The semiconductor device of claim 1, wherein said spacer layer comprises a material that will adhere to a surface of said adjacent semiconductor die.

11. The semiconductor device of claim 1, wherein said spacer layer comprises a polymer.

12. The semiconductor device of claim 11, wherein said polymer comprises a photoimageable polymer.

13. The semiconductor device of claim 1, wherein said spacer layer comprises at least one of a glass, a silicon dioxide, a silicon nitride, and a silicon oxynitride.

17. The semiconductor device of claim 1, further comprising:
adhesive material on an exposed surface of said spacer layer.

18. The semiconductor device of claim 1, wherein said spacer layer comprises a plurality of at least partially superimposed, contiguous, adhered sublayers.

19. (Amended) A semiconductor device assembly, comprising:
a first semiconductor device;
A2 a nonconfluent spacer layer comprising dielectric material and being positioned on a surface of said first semiconductor device; and
a second semiconductor device positioned over said first semiconductor device, a surface of said second semiconductor device being adhered to said nonconfluent spacer layer.

20. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises at least one void therein that communicates with a lateral periphery of said nonconfluent spacer layer.

21. The semiconductor device assembly of claim 20, wherein said at least one void facilitates lateral introduction of adhesive material between said first and second semiconductor devices.

22. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises a plurality of laterally discrete spacers.

23. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer has a substantially uniform thickness.

24. The semiconductor device assembly of claim 19, further comprising:

at least one discrete conductive element protruding above a surface of at least one of said first and second semiconductor devices and located at least partially between said first and second semiconductor devices.

25. The semiconductor device assembly of claim 24, wherein said nonconfluent spacer layer has a thickness that spaces said first and second semiconductor devices apart from one another a distance that exceeds a height said at least one discrete conductive element protrudes above said surface of at least one of said first and second semiconductor devices.

26. The semiconductor device assembly of claim 24, wherein said nonconfluent spacer layer has a thickness that spaces said first and second semiconductor devices apart from one another a distance that is about the same as or less than a height said at least one discrete conductive element protrudes above said surface of at least one of said first and second semiconductor devices.

31. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises a plurality of at least partially superimposed, contiguous, mutually adhered sublayers.

32. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises at least one of a glass, a silicon oxide, a silicon nitride, and a silicon oxynitride.

33. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises a pattern.

37. The semiconductor device assembly of claim 19, further comprising:
a substrate upon which one of said first semiconductor device and said second semiconductor device is positioned.

38. The semiconductor device assembly of claim 37, wherein at least one bond pad of at least one of said first semiconductor device and said second semiconductor device is in communication with a corresponding contact area of said substrate.

39. The semiconductor device assembly of claim 37, wherein said substrate comprises at least one of a circuit board, an interposer, another semiconductor device, and leads.

40. The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer is positioned between an active surface of said first semiconductor device and a back side of said second semiconductor device.

42. The semiconductor device assembly of claim 19, further comprising:
a plurality of nonconfluent spacer layers between said first and second semiconductor devices, additive thicknesses of said plurality of nonconfluent spacer layers defining a distance said first and second semiconductor devices are spaced apart from one another.

43. The semiconductor device assembly of claim 42, wherein a first nonconfluent spacer layer of said plurality of nonconfluent spacer layers is secured to a surface of said first semiconductor device and a second nonconfluent spacer layer of said plurality of nonconfluent spacer layers is secured to an opposed surface of said second semiconductor device.

44. The semiconductor device assembly of claim 42, wherein at least some solid regions of each of said plurality of nonconfluent spacer layers are at least partially superimposed relative to one another.